REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 2-3, 5-9 and 12-16 remain pending in the application. Claims 10-11 have been withdrawn from consideration following a restriction requirement.

Submitted herewith is a Request for Approval of Drawing Changes which addresses the objection of Figure 1 contained in numbered paragraph 4 of the Office Action. Approval of the proposed drawing change is respectfully requested.

In numbered paragraph 5 of the Office Action, claims 4-6 are rejected under 35 U.S.C. § 112, second paragraph. The Office Action alleges that the claims are "indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Claim 4 has been canceled rendering the rejection of claim 4 moot. This rejection with regard to claims 5 and 6 is respectfully traversed.

The specification discusses advantages of providing multiple intersections of ground interconnects in paragraph [0024]. The specification discusses the electrical circuit of Figure 2 and the arrangement of interconnects of Figure 1 at paragraphs [0025] and [0026]. For example, paragraph [0024] discloses that the interconnects 104, 106 of the via 100 afford flexibility in design and placement of electrical features on circuit boards. Paragraphs [0025] and [0026] disclose arrangements of interconnects such that inductance is essentially canceled and the voltage drop approaches zero. Electrically, the signal current and the ground current can, in exemplary embodiments, be routed as close as possible to provide the electrical coupling.

Applicant respectfully asserts that claims 5 and 6 comply with 35 U.S.C. § 112, second paragraph, because they set definite boundaries on the patent protection being sought. Specifically, claim 5 recites that a series ground inductance present in the signal net carried on the first interconnect is essentially canceled by the ground of the circuit carried on the second interconnect. And recited in claim 6, the second interconnect is electrically connected to the ground of the circuit such that a voltage drop of the circuit approaches zero. Claims 5 and 6 fairly convey to a person of ordinary skill in the pertinent art structural attributes of the via claimed in the present application. Thus, applying MPEP § 2173.05(g), claims 5 and 6 comply with 35 U.S.C. § 112, second paragraph. Accordingly, Applicant respectfully requests that this rejection of claims 5 and 6 be withdrawn.

In numbered paragraph 7, claims 1-7 and 9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent JP 404062894A (JP '894). This rejection is respectfully traversed, as the JP '894 patent relied upon by the Examiner does not disclose Applicant's claim 12 via.

The present invention is directed to interconnecting two or more signal layers of a multilayer printed circuit board while maintaining a well coupled signal return back path to reduce signal noise. Figure 1 shows an exemplary embodiment of a via 100 in a printed circuit board 102 having a circuit. The printed circuit board has multiple interleaved layers 112. Some of these layers 112 are used to carry signal current of signal nets 114, while other ones of layers 112 are used as ground planes 116. In the Figure 1 example, two of the layers 112 carrying signal nets 114 connect with first electrical interconnect 104. The layers carrying ground planes 116 connect with second electrical interconnect 106. In the Figure 1 example,

the first interconnect 104 is represented as an inner concentric cylinder and the second interconnect 106 is represented as an outer concentric cylinder. Both the first interconnect 104 and the second interconnect 106 intersect multiple layers of the printed circuit board as shown in Figure 1 and described in paragraph [0024]. Further, the first interconnect and the second interconnect are inductively coupled through the proximity of the first interconnect to the second interconnect in the via. Coupling is discussed, for example, at paragraphs [0020] and [0024] to [0027].

The foregoing features are broadly encompassed by independent claim 12, which is directed to a via for use in a multilayer printed circuit board having a circuit, the printed circuit board including a first plurality of conductive layers and a second plurality of conductive layers, the first and second plurality of conductive layers being interleaved in a first direction which extends parallel to an axis of the via. The via comprises a first interconnect located about the axis of the via and electrically connecting the first plurality of conductive layers to a signal net of the circuit and a second interconnect having a portion located about the first interconnect for electrically connecting the second plurality of conductive layers to a ground plane of the circuit. The second interconnect is coaxial with the first interconnect and is inductively coupled with the first interconnect.

In contrast, JP '894 does not disclose, teach or suggest a via electrically connecting the first plurality of conductive layers to a signal net of the circuit and a second interconnect having a portion located about the first interconnect for electrically connecting the second plurality of conductive layers to a ground plane of the circuit as claimed in claim 12. The via of Figure 1 of JP '894, discloses through-hole copper plating 1 on the circumference surface

of the hole. An inner layer copper foil 5 is provided for a ground circuit and is illustrated abutting a shield plating layer 2. However, the coaxial structure of JP '894 does not show interleaved pluralities of conductive layers either connected to a signal net of the circuit or to a ground plane of the circuit as claimed in claim 12. For at least this reason, an anticipatory rejection of claim 12 is improper since JP '894 does not disclose the invention as claimed.

In addition, JP '894 does not teach or suggest connecting a first and second plurality of conductive layers as claimed in claim 12. For example, even if the structure of JP '894 were to be stacked successively on top of each other to obtain multiple stacked layers, the arrangement of the shield plating layer 2 and inner layer copper foil 5 of JP '894 would not result in connecting a first and second plurality of layers as claimed in claim 12. Nor is there any structural feature of the interconnect of JP '894 that would allow the inner layer copper foil 5 of one layer to be connected to a second inner layer copper foil of an abutting or stacked structure. Thus, for at least this additional reason, the rejection based on the disclosure in JP '894 should be withdrawn.

In numbered paragraph 9 of the Official Action, claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over JP '894 and further in view of U.S. Patent No. 5,876,842, issued to Duffy et al. (hereafter "*Duffy et al.*"). This rejection is respectfully traversed.

Duffy et al. discloses electronic circuit packages having multilayer electrical interconnection patterns. As disclosed in, for example, Figures 2C and 3A and 3B and described in column 8, electrical interconnections can be made between conductors 18 within the vias 15. As shown, the ground is on the metallic foil sheet 12 which is separated from the conductor 18 by dielectric layer 14. In Figure 2C and Figures 3A and 3B, multiple layers are

shown at a single interconnect. However, the metallic foil sheet 12 of each layer is independent and not interconnected. Thus, *Duffy et al.* fails to disclose, teach, or suggest interconnecting ground planes between a plurality of layers as presented in claim 12.

Neither JP '894 nor *Duffy et al.* disclose connecting a first plurality of conductive layers carrying a signal net of the circuit and a second plurality of conductive layers carrying a ground plane of the circuit as claimed in claim 12. Thus, the combination of JP '894 and *Duffy et al.* in the manner relied upon by the Examiner would not have resulted in Applicant's presently claimed invention.

The specification discloses several advantages for interconnecting a ground plane at the via. These include affording circuit designer greater flexibility in the design and placement of electrical features by connecting the layers that are available to carry the induced ground planes. See specification paragraph [0024]. This is in contrast to the use of a typical DIP-type part being inserted in a through-hole in a printed circuit to join ground planes. See specification paragraph [0008]. The concentric first and second interconnect inductively coupled over their length within the via has performance advantages over the "stitched together" approach of the prior art in that the ground plane in the present invention is more intimately coupled with the signal net of the electrical circuit, essentially canceling the inductance and having the voltage drop approach zero. See specification paragraphs [0025] to [0027].

In summary, there is no disclosure, teaching or suggestion in the disclosure of JP '894 or *Duffy et al.* regardless of whether these documents are considered individually or in combination, for a via having the claimed arrangement of features as presented in Applicant's

independent claim 12. Accordingly, claim 12 is allowable. The remaining claims 2-3 and 5-9 depend from claim and recite additional advantageous features which further distinguish over the cited references. These dependent claims are also considered allowable.

New claims 13-15 define further distinguishing characteristics associated with the claimed via. Claim 13 recites that the first interconnect has a length that is coextensive in length with the via. Claim 14 recites that the second interconnect has a length that is no more than the length of the first interconnect and that the second interconnect is parallel to the first interconnect along an entire length of the second interconnect. Finally, claim 15 recites that the entire length of the second interconnect is in one plane. The interconnect of dependent claims 13-15 distinguishes over the cited references for at least the same reasons as discussed above. Accordingly, these new claims are considered allowable. Support for these new claims can be found, for example, in at least Applicant's Figure 1.

New claim 16 is directed to a multilayer printed circuit board having a circuit. Claim 16 recites that the multilayer printed circuit board comprises a first plurality of conductive layers, a second plurality of conductive layers, the first and second plurality of conductive layers being interleaved in a first direction which extends parallel to an axis of the via, and a via. The via includes a first interconnect, the first interconnect located about the axis of the via and electrically connecting the first plurality of conductive layers to a signal net of the circuit, and a second interconnect, the second interconnect located about at least a portion of the first interconnect and electrically connecting the second plurality of conductive layers to a ground plane of the circuit. The second interconnect is coaxial with the first interconnect along its length in the first direction and is inductively coupled with the first interconnect.

a plurality of electrically conductive layers and a plurality of dielectric layers. At least one dielectric layer separates any two consecutive conductive layers in a first direction. The multilayer printed circuit board also includes a via. The arrangement of the claimed printed circuit board is different than that disclosed in either JP '849 or *Duffy et al.*, in that the via includes a first and a second interconnect where the first interconnect is located about the axis of the via and electrically connects the first plurality of conductive layers to a signal net of the circuit, and the second interconnect is located about at least a portion of the first interconnect and electrically connects the second plurality of conductive layers to a ground plane of the circuit. Further, the second interconnect is coaxial with the first interconnect along its length in the first direction and is inductively coupled with the first interconnect. Neither JP '849 nor *Duffy et al.* alone or in combination, disclose, teach, or suggest a multilayer printed circuit board having a circuit with a via having an arrangement of features as presented in claim 16. Accordingly, claim 16 distinguishes over the cited references and is considered allowable. Support for this new claim can be found, for example, in at least Figure 1.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Jeffrey G. Killian
Registration No. 50,891

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

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